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EXAMINER	
CHOW, CHARLES CHIANG	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,405	YOUNG ET AL.	
	Examiner	Art Unit	
	Charles Chow	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-12,14,15,17,19-25,27,28,30,32-38 and 40* is/are pending in the application.

4a) Of the above claim(s) *3,5,13,16,18,26,29,31 and 39* is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *1,2,4,6-12,14,15,17,19-25,27,28,30 and 32-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This office action is for amendment dated 10/25/2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 6-8, 12, 27-28, 30, 32-34, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (US 6,498,927B2) in view of Sullivan (US 5,451,955).

For claim 1, Kang et al. [hereafter as Kang] teaches a method [steps in Fig. 9] for processing received signals in a communication system [the processing received signals by antenna 802 in wireless system 800 in Fig. 8 & abstract, the dynamic range in col. 9, lines 11-22], the method comprising

generating a plurality of upstream analog signals for a received signal [the down converted signal are output at each VGA of the plural variable gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62; as the plural upstream analog signals];

adjusting a gain for said received signal using computed power [monitoring the power level in col. 9, lines 5-22 & Fig. 9, col. 9, lines 30-37; the reducing the gain of the selected stage, col. 9, lines 34-67 & the increasing the gain in col. 11, lines 24-37].

Kang fails to teach the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals; computing a power of said received signal based on said plurality of corresponding digital signals.

Sullivan teaches the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals [the quantizer 10 comprising plurality of converting element 20 with ADC 28 for converting detected power level into digital signal, for amplifier stages 12-18 serially connected, Fig. 1, col. 5, lines 12-59, to convert upstream narrow band analog signals of a channel into plurality of corresponding digital signals],

the computing a power of said received signal based on said plurality of corresponding digital signals [the computing power of received signal by combining the latched portions of each digital power level of stage A to stage D, Fig. 1, col. 5, lines 56-59, & provide the measured power level of rf signal, as shown in table 2, col. 7, lines 16-39 & col. 7, line 6 to col. 8, line 11], for accurately control the amplified rf signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Sullivan's plurality of ADC 28 in sequence for converting detected power level, in order to accurately control the amplified rf signal.

For claims 2, 28, Kang further teaches the comprising low pass filtering said received signal [the base band BB filter 852 is low pass filtering of received signal, to reduce SNR degradation in Fig. 8, col. 8, lines 56-62].

For claims 4, 30, Kang teaches the further comprising acquiring at least one sample from at least a portion said generated plurality of upstream analog signals [the measuring power in step s910 & the power detecting power level at PD 820-868 of amplified signal at each VGA output, col. 9, lines 5-22; the received by gain controller 894 & AGC 884 via 876, as the processor]. Sullivan teaches the acquiring at least one digital sample from at least a portion said plurality of corresponding digital signals [ADC 28 in Fig. 1 providing at least one digital representation of the sampled portion].

For claims 6, 32, Kang teaches the further comprising determining when at least one of said generated plurality of upstream narrow band analog signals is clipped [the base band filters 836, 852 provides the upstream narrow band analog signal in col. 8, col. 46-62; the above upper limit of signal level 1020, clipped, the gain controller, as processor, decreases the gain, col. 10, lines 48-58, Fig. 10B].

For claims 7, 33, Kang teaches the further comprising generating an intermediate gain based on said computed power of said acquired at least one sample [the intermediate gain change in steps s940 or s950, then process looping upwards to S910, before final gain, Fig. 9].

For claims 8, 34, Kang teaches the further comprising applying said generated intermediate gain to said at least one of said generated plurality of upstream narrow band analog signals [the reducing the gain stage by predetermined gain step size at s940, s950, Fig. 9, as the applying said intermediate gain; the base band filters 836, 852 provides the upstream narrow band analog signal in col. 8, col. 46-62].

For claims 12, 38, Kang fail to teach the features for this claim. Sullivan teaches the comprising applying a final gain to said received signal, wherein said final gain is applied after processing signals upon which intermediate gain has been applied [the amplifier 18, as the final gain applied after intermediate gains at amplifiers 12-16, Fig. 1].

For claim 27, Kang teaches a system for processing received signals in a communication system [the signal received by antenna 802 in wireless system 800 in Fig. 8 & abstract, the dynamic range in col. 9, lines 11-22], the system comprising

a receiver [803] that generates a plurality of upstream narrow band analog signals for a received signal [the down converted signal are output at each VGA of the plural variable

gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62; the base band filters 836, 852 generates plurality of upstream narrow band analog signal in col. 8, col. 46-62];

at least one automatic gain controller [828, col. 9, line 37] that adjusts a gain for said received signal using at least a portion of said analog information [the reducing the gain of the selected stage, col. 9, lines 34-67 & increasing the gain col. 11, lines 24-37].

Kang fails to teach a plurality of analog to digital converters that convert at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals; at least on processor that computes power of said received signal based on said plurality of corresponding digital signals.

Sullivan teaches a plurality of analog to digital converters that convert at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals [the quantizer 10 comprising plurality of converting element 20 with ADC 28 for converting detected power level into digital signal, for amplifier stages 12-18 serially connected, Fig. 1, col. 5, lines 12-59, to convert upstream narrow band analog signals of a channel into plurality of corresponding digital signals],

at least one processor [prom 30-34, latch 36-40] that computes power of said received signal based on said plurality of corresponding digital signals [the computing power of received signal by combining the latched portions of each digital power level of stage A to stage D, Fig. 1, col. 5, lines 56-59, & provide the measured power level of rf signal, as shown in table 2, col. 7, lines 16-39 & col. 7, line 6 to col. 8, line 11], for accurately control the amplified rf signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Sullivan's plurality of ADC 28 in sequence for converting detected power level, in order to accurately control the amplified rf signal.

4. Claims 9-11, 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Sullivan, as applied to claims 1, 27 above, and further in view of Brobston et al. (US 7,031,409 B2).

For claims 9, 35, Kang teaches the computing the accurate rssi 892, Kang, Sullivan fail to teach the comparing with defined power values.

Brobston et al. [Brobston] teaches the comparing said computed power to a plurality of defined power values [the computed power sample from output of 333 is compared with the program threshold value in register 335 at 341, the program threshold values are the defined power values; to determined the saturation at 342, for controlling the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37, the agc for dynamic range in abstract, title], the agc 215 is processor controlled FPGA device [col. 7, lines 40-45] & with software programmability [col. 12, lines 30-32]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Sullivan with Brobston's comparing the calculated power samples to the threshold value, in order to determine & reduce signal saturation.

For claims 10, 36, Kang teaches the computing the accurate rssi 892, Kang, Sullivan fail to teach the selecting a gain based on a comparable power value of said plurality of defined power values.

Brobston teaches the selecting a gain based on a comparable power value of said plurality of defined power values [the computed power sample at the output of 333 with the program threshold value in register 335 at 341, the program threshold values are the defined power values; to determined the saturation at 342, for controlling the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37]; the agc 215 is a processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software

programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang, Sullivan.

For claims 11, 37, Kang teaches the computing the accurate rssi 892, Kang, Sullivan fail to teach the storing said defined power values in a lookup table. Brobston teaches the programmable threshold values are stored in the register 335 as the lookup table [col. 8, lines 27-27]; the agc 215 is a processor controlled FPGA device, as the code control process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang, Sullivan.

7. Claims 14, 17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Sullivan and Oschima (US 2003/0218,501 A1).

For claim 14, Kang teaches the steps in Fig. 9, Fig. 11, comprising

generating a plurality of upstream analog signals for a received signal [the down converted signal are output at each VGA of the plural variable gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62; as the plural upstream analog signals];

adjusting a gain for said received signal using computed power [monitoring the power level in col. 9, lines 5-22 & Fig. 9, col. 9, lines 30-37; the reducing the gain of the selected stage, col. 9, lines 34-67 & the increasing the gain in col. 11, lines 24-37].

Kang fails to teach the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals; computing a power of said received signal based on said plurality of corresponding digital signals.

Sullivan teaches the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals

[the quantizer 10 comprising plurality of converting element 20 with ADC 28 for converting detected power level into digital signal, for amplifier stages 12-18 serially connected, Fig. 1, col. 5, lines 12-59, to convert upstream narrow band analog signals of a channel into plurality of corresponding digital signals],

the computing a power of said received signal based on said plurality of corresponding digital signals [the computing power of received signal by combining the latched portions of each digital power level of stage A to stage D, Fig. 1, col. 5, lines 56-59, & provide the measured power level of rf signal, as shown in table 2, col. 7, lines 16-39 & col. 7, line 6 to col. 8, line 11], for accurately control the amplified rf signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Sullivan's plurality of ADC 28 in sequence for converting detected power level, in order to accurately control the amplified rf signal.

Kang teaches the processor executed code section for the steps in Fig. 9, Fig. 11. Kang & Sullivan fail to mention the computer program stored in a machine readable storage, for processing signals with the executable code section.

Oschima et al. [Oschima] teaches a machine-readable storage having stored thereon, a computer program having at least one code section for processing received signals in a communication system, the at least one code section being executable by a machine for causing the machine to perform steps [the computer or microprocessor executes instructions stored program software for implementing the gain control method, in paragraph 0068-0070 & gain method in abstract], in order to accurately control the amplifier gain by executing software instructions. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Sullivan with Oschima's

software instructions, in order to accurately control the amplifier gain by executing software instructions.

For claim 17, Oschima teaches the machine-readable storage having stored computer program in claim 14 above. Kang teaches the further comprising code for acquiring at least one sample from at least a portion said generated plurality of upstream analog signals [the measuring power in step s910 & the power detecting power level at PD 820-868 of amplified signal at each VGA output, col. 9, lines 5-22; the received by gain controller 894 & AGC 884 via 876, as the processor], Sullivan teaches the at least one digital sample from at least a portion said plurality of corresponding digital signals [the plurality of ADC 28 for generating digital samples of the corresponding portion, Fig. 1] using the same reasoning in claim 14 above to combine Oschima to Kang, Sullivan.

For claim 19, Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the determining when at least one of said generated plurality of upstream narrow band analog signals is clipped [the base band filters 836, 852 provides the upstream narrow band analog signal in col. 8, col. 46-62; the above upper limit of signal level 1020, clipped, the gain controller, as processor, decreases the gain, col. 10, lines 48-58, Fig. 10B], using the same reasoning in claim 14 above to combine Oschima to Kang, Sullivan.

For claim 20. Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the generating an intermediate gain based on said computed power [the intermediate gain change in steps s940 or s950, then process looping upwards to S910, before final gain, Fig. 9], using the same reasoning in claim 14 above to combine Oschima to Kang, Sullivan.

For claim 21, Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the applying said generated intermediate gain to said at least one of said generated plurality of upstream narrow band analog signals [the base band filters 836, 852 provides the upstream narrow band analog signal in col. 8, col. 46-62; the reducing the gain stage by predetermined gain step size at s940, s950, Fig. 9, as the applying said intermediate gain], using the same reasoning in claim 14 above to combine Oschima to Kang.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Sullivan, Oschima, as applied to claim 14 above, and further in view of Loper (US 5,095,536).

For claim 15, Kang, Sullivan fail to teach the features for this claim.

Oschima teaches the machine-readable storage having stored computer program in claim 14 above. It is well known that the low pass filter can be implemented in by software coding, such as the teaching from Loper, the FIR filter in the digital signal processing [col. 12, lines 43-58]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Sullivan, Oschima with Loper's FIR low pass filtering, such that the low pass filter could be convenient relocated for the purpose of processing a signal.

10. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Sullivan, Oschima, as applied to claim 14 above, and further in view of Brobston-'409B2.

For claims 22, 23, Kang, Sullivan & Oshima fail to teach the code for comparing said computed power to a plurality of defined power values; the code for selecting gain based on a comparable power value of said plurality of defined power values.

Brobston teaches these features [the computed power sample from output of 333 is compared with the program threshold value in register 335 at 341, the programmable threshold values are the defined power values; to determined the saturation at 342, for controlling, selecting, the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37; the agc for dynamic range in abstract, title], the agc 215 is the processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Sullivan, Oshima with Brobston's comparing the calculated power samples to the threshold value, in order to determine & reduce signal saturation.

For claim 24, Kang, Sullivan & Oshima fail to teach the code for storing said defined power value in a lookup table.

Brobston teaches these features [the programmable threshold values are stored in the register 335 as the lookup table in col. 8, lines 27-27]; the agc 215 is a processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang, Sullivan & Oshima.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Sullivan, Oshima-501A1, as applied to claim 14 above, and further in view of Oshima-'586A1.

For claim 25, Kang fails to teach the features for this claim. Sulivan teaches the applying a final gain to said received signal, wherein said final gain is applied after processing signals upon which intermediate gain has been applied [the amplifier 18, as the final gain applied after intermediate gains at amplifiers 12-16, Fig. 1].

Sullivan fails to teach the machine readable storage comprising code for applying final gain.

Oshima-586A1 teaches the code for applying a final gain to said received signal [the applying of the final gain code FGC & generating the gain control information based on the difference, 0061-0062, Fig. 19], for accurately control the rest of the gain value based on the preceding gain stage. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Sullivan, Oshima-501A1 with Oshima-586A1's final gain code, in order to accurately control the rest of the gain value based on the preceding gain stage.

Allowable Subject Matter

12. The following is an examiner's statement of reasons for allowance:

Claim 40 is allowable over the prior art of record. The prior arts fail to teach the allowable features, singly, particularly, or in combination.

The cited prior arts fail to teach the structure that **an input of a first of said plurality of analog-to-digital converters is directly electrically coupled to said output pf said low pass filter**, together with a low pass filer directly electrically coupled to said mixer; and an input of each of a remaining portion of said plurality of analog to digital converters is individually directly electrically coupled to a corresponding output of each of sad serially coupled plurality of gain controllers.

The closest prior art **Sullivan (US 5,451,955)** teaches plurality of ADC 20 for the sequentially connected gain stages 12-16, the ADC 20 are coupled to the amplifier gain stages 12-16 via couplers 22, diode 24, amplifier 26, Fig. 1, which is not directly electrically coupled to the amplifiers.

Ichihara (US 2001/0022,821 A1) teaches the band pass filter 5 which is directly connected to mixer 32 [Fig. 1] for the amplitude deviation controlling [abstract].

Wada et al. (US 6,304,206 B1) teaches the ADC converters 309 directly connected to the operational amplifiers 302, 311a-313 in Fig. 1.

Other prior arts in below were also considered, but they fail to teach the above allowable features. They are as follows:

Kang (US 6,498,927 B2), Brobston et al..)US 7,031,409 B2), Sochima (US 2003/0218,501 A1), Loper (US 5,095,536).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Argument

13. Applicant's arguments with respect to claims 1-2, 4, 6-12, 14-15, 17, 19-25, 27-28, 30, 32-38 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant argument for the no teachings of the features,

the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals; the computing a power of said received signal based on said plurality of corresponding digital signals.

Sullivan (US 5,451, 955) teaches the converting at least two of said generated plurality of upstream narrow band analog signals for a channel to a plurality of corresponding digital signals [the quantizer 10 comprising plurality of converting element 20 with ADC 28 for converting detected power level into digital signal, for amplifier stages 12-18 serially connected, Fig. 1, col. 5, lines 12-59, to convert upstream narrow band analog signals of a channel into plurality of corresponding digital signals],

the computing a power of said received signal based on said plurality of corresponding digital signals [the computing power of received signal by combining the latched portions of each digital power level of stage A to stage D, Fig. 1, col. 5, lines 56-59, & provide the measured power level of rf signal, as shown in table 2, col. 7, lines 16-39 & col. 7, line 6 to col. 8, line 11].

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow CC

November 30, 2006.